I claim:

1. An apparatus, comprising:

execution logic to execute a load instruction with a predicted load value; and

a table coupled to the execution logic and having a first field to store the predicted load value, the table to be used in repairing a mis-prediction of the predicted load value after a cache miss caused by a request of an actual load value.

2. The apparatus of claim 1, wherein:

the execution logic is to execute the load instruction with the actual load value responsive to a cache hit caused by execution of the load instruction.

3. The apparatus of claim 1, wherein:

the table includes a miss status holding register.

4. The apparatus of claim 1, wherein:

the table includes a second field to indicate a destination register for the load instruction.

5. The apparatus of claim 1, wherein:

the table includes a second field to store an address identifying a location of the actual load value.

6. A system, comprising:

a main memory;

a cache memory coupled to the main memory;

instruction execution logic coupled to the cache memory to execute a load instruction with an actual load value if a request of the actual load value results in a cache hit and to execute the load instruction with a predicted load value if the request of the actual load value results in a cache miss; and

a table coupled to the instruction execution logic and having a first field to store the predicted load value if the request of the actual load value results in the cache miss.

7. The system of claim 6, wherein:

the table includes a miss status holding register.

8. The system of claim 6, wherein:

the instruction execution logic is further to execute a check instruction to compare the predicted load value from the first field with the actual load value.

9. The system of claim 8, wherein:

the instruction execution logic is further to branch to repair code if the predicted load value is different than the actual load value.

10. The system of claim 6, wherein:
the table is to not store the predicted load value if the request for the actual load value results in the cache hit.

11. An apparatus, comprising:
a processor to execute an instruction set including
a first set of one or more instructions to load a predicted load value and to place the predicted load value in a table in response to an attempt to load an actual load value resulting in a cache miss; and
a second set of one or more instructions to compare the predicted load value from the table with the actual load value and branch to repair code if the actual load value is different than the predicted load value.

12. The apparatus of claim 11, wherein:
the first set is to not place the predicted load value in the table in response to the attempt to load the actual load value resulting in a cache hit.

13. The apparatus of claim 11, wherein:
the second set is to examine the table to determine if the table includes the predicted load value.

14. The apparatus of claim 11, wherein:
the first and second sets are to be specified by a compiler.

15. The apparatus of claim 11, wherein:
the first and second sets are to be specified during execution.

16. A method, comprising:
executing a load instruction using a predicted load value responsive to a cache miss resulting from an attempt to execute the load instruction with an actual load value;
placing the predicted load value in a table;
retrieving the actual load value;
comparing the actual load value with the predicted load value in the table to determine if the predicted load value was mis-predicted; and
re-executing at least one of the load instruction and load-dependent instructions using the actual load value if the predicted load value was mis-predicted.

17. The method of claim 16, wherein:
said comparing includes comparing after the load instruction is retired.

18. The method of claim 16, wherein:
said placing includes placing the predicted load value in a miss status holding register.

19. A machine-readable medium that provides instructions, which when executed by a set of one or more processors, cause said set of processors to perform operations comprising:

executing a load instruction using a predicted load value responsive to a cache miss resulting from an attempt to execute the load instruction with an actual load value;

placing the predicted load value in a table if said attempt results in a cache miss;

comparing the actual load value with the predicted load value from the table to determine if the predicted load value was mis-predicted; and

re-executing at least one of the load instruction and load-dependent instructions using the actual load value if the predicted load value was mis-predicted.

20. The medium of claim 19, wherein:

said re-executing includes branching to repair code.

21. The medium of claim 19, wherein:

said comparing includes determining if the table includes an entry corresponding to the load instruction.

22. The medium of claim 19, wherein:

said placing includes placing the predicted load value in a miss status holding register.

23. A method, comprising:

generating first code to load an actual load value if requesting the actual load value results in a cache hit, and to load a predicted load value and place the predicted load value in a table if requesting the actual load value results in a cache miss;

generating second code to compare the predicted load value from the table with the actual load value; and

generating third code to execute at least one of a load instruction and a load-dependent instruction with the actual load value.

24. The method of claim 23, wherein:

said generating the second code includes generating code to determine if the table includes an entry generated by the first code.

25. The method of claim 23, wherein:

said generating the third code includes generating code to be executed if executing the second code determines the predicted load value is different than the actual load value.

26. The method of claim 23, further comprising:

generating said first, second, and third code only if it is determined that said requesting the actual load value is likely to result in a cache miss.

27. A machine-readable medium that provides instructions, which when executed by a set of one or more processors, cause said set of processors to perform operations comprising:

generating first code to load an actual load value if requesting the actual load value results in a cache hit, and to load a predicted load value and place the predicted load value in a table if requesting the actual load value results in a cache miss;

generating second code to compare the predicted load value from the table with the actual load value; and

generating third code to execute at least one of a load instruction and a load-dependent instruction with the actual load value.

28. The medium of claim 27, wherein:

said generating the second code includes generating code to determine if the table includes an entry generated by the first code.

29. The medium of claim 27, wherein:

said generating the third code includes generating code to be executed if executing the second code determines the predicted load value is different than the actual load value.

30. The medium of claim 27, further comprising:

generating said first, second, and third code only if it is determined that said requesting the actual load value is likely to result in a cache miss.